

Bridgeless Quadratic Buck Converter With High Step-down Capability for Energy Harvesting Applications

Zhengge Chen^{†,‡}, Member, IEEE, Jianping Xu[†], Member, IEEE, Jiheng Cai[†], Yuxin Liu[‡], Student Member, IEEE, and Tianci Wang[‡], Student Member, IEEE

[†]School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China
zgc@swjtu.edu.cn, jpxu@swjtu.edu.cn, cjh13456391782@163.com

[‡]School of Energy and Environment, City University of Hong Kong, Hong Kong, China
zhengge.chen@cityu.edu.cn, yuxin.liu@my.cityu.edu.hk, tianci.wang@my.cityu.edu.hk

Abstract—In energy harvesting, triboelectric nanogenerator (TENG) exhibits the great potential capability of scavenging the environmental kinetic energy into power electricity, which can be a promising distributed power source for an Internet of Things (IoTs) device. However, those TENGs usually generate very high output voltage for the post-stage interface circuit, and thus a high step-down AC-DC converter for efficient power conversion is necessary. This paper proposes two bridgeless quadratic buck AC-DC topologies for high-voltage step-down. Then, one of the proposed topologies is analyzed with its operation modes and voltage ratio between input and output. The simulation results validate the topology feasibility and analysis correctness.

Index Terms—energy harvesting, distributed power source, bridgeless quadratic buck, high step-down

I. INTRODUCTION

By 2024, Wireless sensor nodes (WSNs) are predicted to grow more than threefold compared with that given in 2019 [1]. This phenomenon is attributed to the digitalization requirements of our physical world for a more intelligent society with the help of artificial intelligence (AI). Through these digital twins, which reflect the physical parameters in our real world, more advanced control methods, precise sensing technology, in-time monitoring, and Internet of things can be possibly carried out by AI models and be accessible for our daily usages [2], [3].

Those WSNs, as bridges to connect the physical and digital worlds, are important in the processing of digitalizing our world. However, these WSNs are sometimes installed in harsh environments without easy access to the cable power supply. For example, they can be located in wind turbine blade [4], the human body [5], the high speed train railway [6], ocean light beacon [7], pipeline of petrol supply chain [8], and so on. Thus, a distributed wireless power source based on the energy harvesting (EH) for those WSNs can be a promising solution.

A triboelectric nanogenerator (TENG) mainly relies on the contact charging and tight electrostatic coupling between

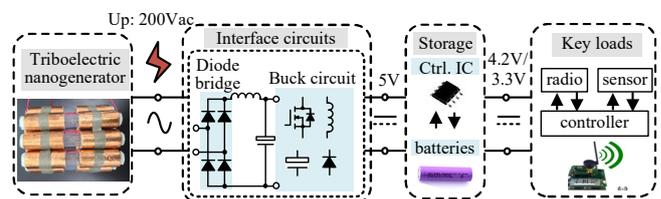


Fig. 1. High step-down AC-DC converters required by WSN applications

various materials to generate electricity [9]. TENG can have a flexible size with a simple structure to fit itself into different operating conditions, which becomes a cost-effect hot topic of the wireless power source for WSNs [10], [11]. However, as shown in Fig. 1 TENG's output voltage is typically high, even up to 200Vac, which can raise a power conversion challenge, since the post-stage circuit usually operate in a 3.3V or 5V condition. Hence, a high step-down interface circuit is necessary to achieve a high efficient AC-DC power conversion for these applications [12], [13].

Many interface circuits use a diode bridge to transfer AC input to DC output. However, they are considered less efficient compared with the bridgeless circuit [14]. The bridgeless AC-DC converter circuits use dual converter cells to handle the positive and negative AC input respectively. Thus, they do not require a diode bridge to complete the AC-DC conversion [15]–[17]. Several boost bridgeless, buck-boost bridgeless, and buck bridgeless circuits have been already proposed [18]–[20]. However, they are not targeting TENG applications with very high output voltage. A more common solution is just to use two-stage power conversion for the high voltage step-down. A two-stage solution is apparently not energy-effective and size-compact in energy harvesting applications, not to mention that the energy harvested by the TENG is typically low and precious. Hence, based on a single-switch high step-down converter cell (named quadratic buck [21]), this paper proposes high step-down bridgeless circuits for those TENGs with high output voltages.

The remainder of this paper is as follows. Section II introduces the quadratic buck converter cell and its conventional AC-DC circuit topologies with a diode bridge, followed by two proposed circuit topology. Then, one of the proposed

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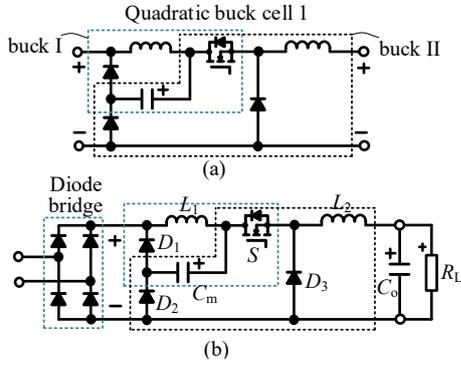


Fig. 2. Quadratic buck AC-DC converter topology. (a) Quadratic buck converter cell and (b) the relative circuit for AC-DC application.

circuit is analyzed with specific operation modes and voltage step-down ratio. Simulation results and the control method are presented in Section III. Finally, the conclusion of this study is drawn in Section IV.

II. PROPOSED HIGH STEP-UP BRIDGELESS CONVERTERS

A. Conventional Quadratic Buck VS. Proposed Ones

Fig. 2 shows the quadratic buck converter cell and its relative circuit for the AC-DC application. As indicated in Fig. 2(a), the quadratic buck converter cell can be considered as a two-stage cascaded buck topology with only a single switch. Compared with the conventional two-stage cascaded buck converters, the quadratic buck converter benefits from a simpler topology structure and reduced switch drive circuit. Theoretically, it can achieve the same voltage step-down ratio as the two-stage cascaded buck converter [21]. Fig. 2(b) shows the corresponding quadratic buck AC-DC converter topology. It relies on a diode bridge to firstly transfer AC to DC and then step down the rectified voltage to a stable output voltage by the quadratic buck circuit. However, it employs two rectifier diodes, which can cause extra conduction loss.

This paper proposes two quadratic buck cell-based bridgeless AC-DC topology circuits, as shown in Fig. 3. Compared with the conventional quadratic buck AC-DC circuit, each proposed topology uses two quadratic buck cells to form a bridgeless circuit and thus a diode bridge is eliminated. As shown in Fig. 3(a) and (b), the proposed topologies are derived by the quadratic buck cell arranged in the input-parallel output parallel (IPOP) and input-parallel output-series (IPOS), respectively.

However, the IPOP quadratic buck converter has a stray current as the same as the IPOP bridgeless buck converter explained in [16]. The main reason is the anti-parallel diode across MOSFET, which offer a unwanted current path. This problem can be actually solved in a near future by the mature technology of a brand-new MOSFET totally without a body diode. Compared with the IPOP topology rival, the IPOS quadratic buck converter has no stray current and thus is studied in the following sections.

B. Proposed Topology Operation Modes

Since the application is energy harvesting and the power processing is relatively low (typical milliwatt to watt level), the discontinuous conduction mode (DCM) of the converter is chosen due to its advantages of low switching loss and simple control method. Figs. 4 and 5 show the IPOS quadratic buck converter operation modes in the positive and negative

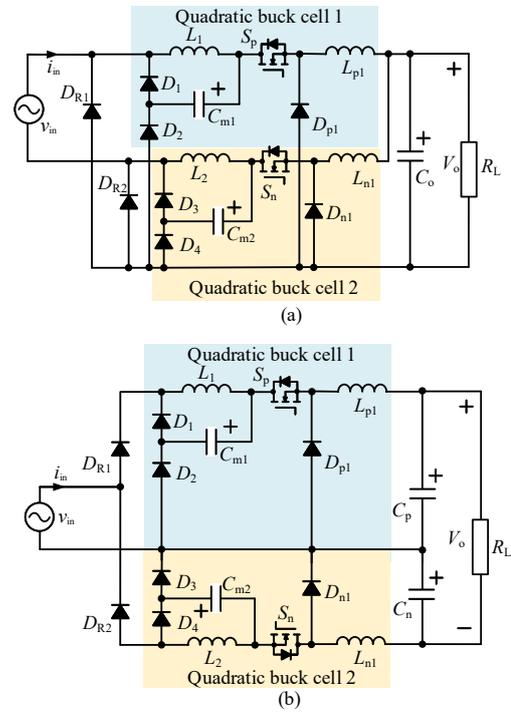


Fig. 3. Proposed bridgeless quadratic buck converters with high step-up voltage ratio. (a) IPOP quadratic buck. (b) IPOS quadratic buck.

AC input cycles, respectively. Due to the similarity of the operation modes in the positive and negative AC input cycles, the following parts only introduce the modes in the positive AC input cycle.

Mode 1: When the switch S_p is turned on, the input AC charges input inductor L_1 and storage inductor L_{p1} via the rectifier diode D_{R1} and switch S_p . The middle capacitor C_{m1} charges storage inductor L_{p1} through diode D_2 . Meanwhile, the output capacitor C_p is charged and C_n discharged. During this period, the currents i_{L1} and i_{Lp1} in the inductors L_1 and L_{p1} increase linearly. The capacitor voltage V_{cm1} across C_{m1} and output voltage V_{cp} across C_p increases. The capacitor voltage V_{cn} across C_n decreases.

Mode 2: When S_p is turned off, the energy stored in the inductor L_1 charges the middle capacitor C_{m1} via diode D_1 . The energy stored in L_{p1} finds its way to charge output capacitor C_p through D_{p1} and support the load R_L . During this period, i_{L1} and i_{Lp1} decrease linearly until to zero. V_{cm1} and V_{cp} increase and V_{cn} decreases.

Mode 3: S_p is in the off-state. i_{L1} and i_{Lp1} keep zero. V_{cm1} remains unchanged. C_p and C_n charge the load R_L . V_{cp} and V_{cn} decrease.

Based on the operation modes, theoretical waveforms of the key components are given in Fig. 6. Since there are two inductors and one switch, one on-time duty cycle d_{on} and two different off-time duty cycles d_{of1} and d_{of2} are in Fig. 6.

C. High Step-Down Voltage Output

In order to analyze the voltage gain of the bridgeless quadratic buck converter, necessary assumptions are given. (1) The switching frequency is much larger than the AC input frequency, and thus $f_s \gg f_L$. (2) The output capacitors and the middle capacitors are large enough and V_{cp} , V_{cn} , V_{cm1} , and V_{cm2} are seen as a constant in switching cycles. (3) The output voltage V_o is much less than the input voltage V_{in} , and thus the AC input dead time can be ignored.

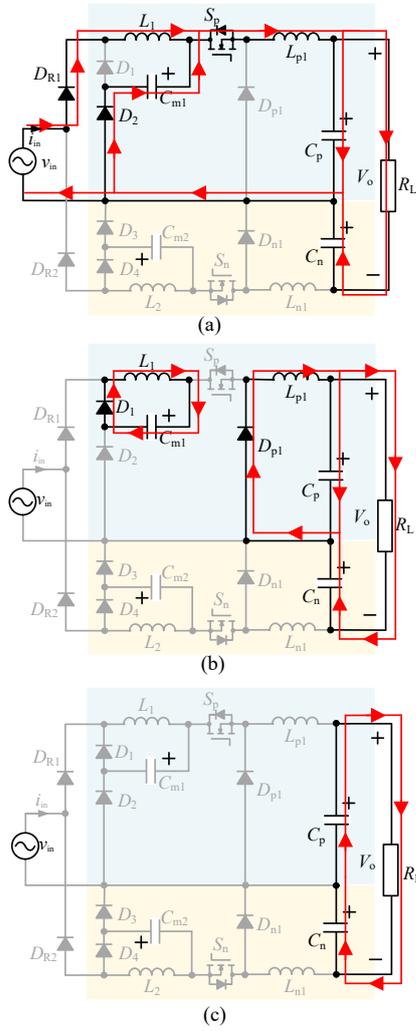


Fig. 4. IPOS quadratic buck converter operation modes in the positive AC input cycle with (a) S_p in ON-state, (b) S_p in OFF-state, and (c) S_p in OFF-state, C_p and C_n support load.

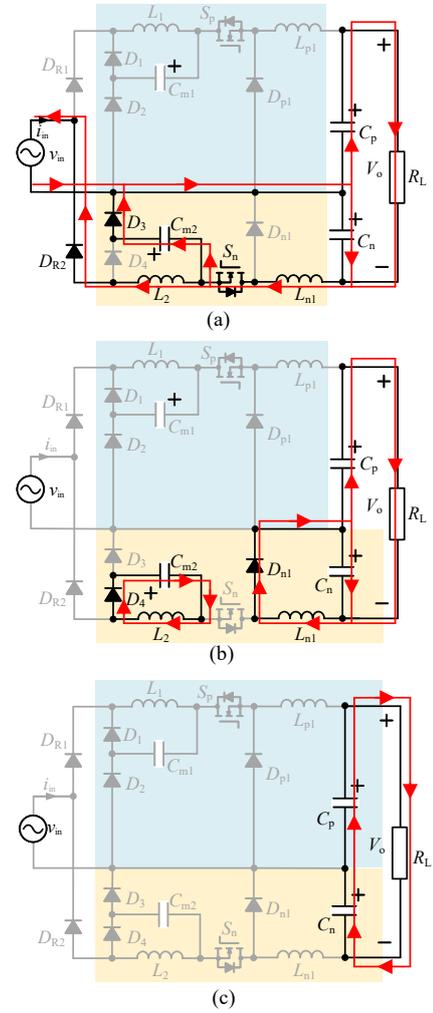


Fig. 5. IPOS quad-boost operation modes in the negative AC input cycle with (a) S_n in ON-state, (b) S_n in OFF-state, and (c) S_n in OFF-state, C_p and C_n support load.

Assuming that the input voltage v_{in} has the peak voltage as V_M and the angular frequency is ω , then it has

$$v_{in}(t) = V_M \sin(\omega t) \quad (1)$$

In one switching cycle, the average input AC current can be seen as the rectifier diode average current $i_{DR1,avg}$, as

$$i_{in} = i_{DR1,avg} = \begin{cases} \frac{[v_{in} \sin(\omega t) - V_{cm1}]d_{on}^2}{2L_1 f_S} & t \in [\frac{\alpha}{\omega}, \frac{\pi-\alpha}{\omega}] \\ 0 & [0, \frac{\alpha}{\omega}] \cup (\frac{\pi-\alpha}{\omega}, \frac{\pi}{\omega}] \end{cases} \quad (2)$$

where $\alpha = \arcsin(V_{cm1}/V_M)$ and f_S is the switching frequency. In the half cycle of the AC input, based on (1) and (2) the input power can be expressed as

$$P_{in} = \frac{2}{T_L} \int_0^{T_L/2} v_{in}(t) i_{in}(t) dt = \frac{V_M^2 d_{on}^2}{2\pi L_1 f_S} [\frac{\pi}{2} - \alpha - m \cos(\alpha)] \quad (3)$$

where $m = V_{cm1}/V_M$ and T_L is an AC input cycle. The output power P_o is

$$P_o = V_o^2 / R_L \quad (4)$$

On the other hand, considering the quadratic buck DC-DC converter operation modes, the middle capacitor C_{m1} can be seen as the cascaded buck converter input voltage V_{cm1} . Thus,

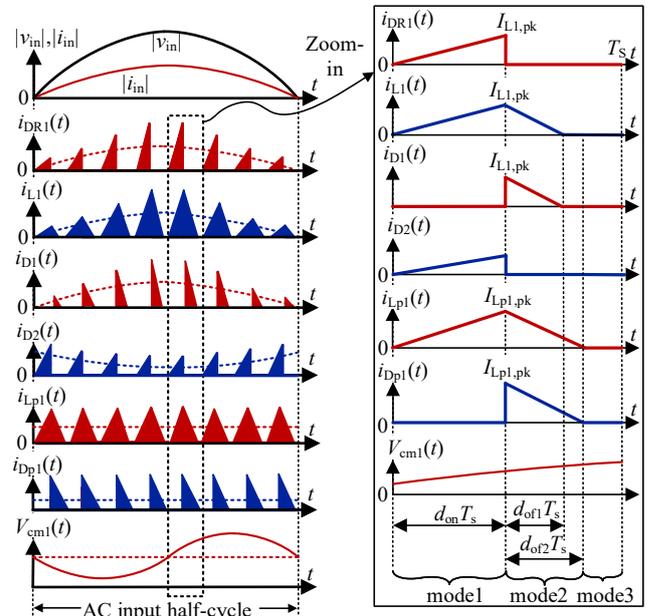


Fig. 6. Key waveforms of the S-IPOP quad-boost converter.

the average current $i_{D2,avg}$ of the diode D_2 is

$$i_{D2,avg} = \frac{(V_{cm1} - V_o/2)d_{on}^2}{2L_{p1}f_S} \quad (5)$$

TABLE I. Design Specifications of Proposed Converter

Symbol	Parameters	Quantity
f_s	Switching frequency	65kHz
f_L	AC input frequency	300Hz
V_M	peak input voltage	200Vac
V_o	Output voltage	5V
$L_1=L_2$	Input inductors	22 μ H
$L_{p1}=L_{n1}$	Storage inductor	3 μ H
$C_{m1}=C_{m2}$	Middle capacitor	200 μ F
$C_p=C_n$	Output capacitor	4000 μ F
R_L	Resistor	2 Ω

The output power of V_{cm1} for the post-stage is

$$P_{out,cm1} = V_{cm1} i_{D2,avg} = \frac{(V_{cm1}^2 - V_{cm1} V_o/2) d_{on}^2}{2L_{p1} f_s} \quad (6)$$

Considering the power balance between the middle capacitor and the final output, it has $P_{out,cm1}=P_o$, which leads to

$$m_2 = \frac{V_{cm1}}{V_o} = \frac{1}{4} + \frac{1}{2} \sqrt{\frac{1}{4} + 4K_1} \quad (7)$$

where $K_1=(2L_{p1}f_s)/(R_L d_{on}^2)$. Combining (3), (4), and (7), it leads to the voltage ratio between V_o and V_M as

$$\frac{\pi}{2} - \arcsin\left(\frac{m_2 V_o}{V_M}\right) - \frac{m_2 V_o}{V_M} \sqrt{1 - \sin^2\left(\frac{m_2 V_o}{V_M}\right)} = \frac{2V_o^2 \pi L_1 f_s}{V_M^2 R_L d_{on}^2} \quad (8)$$

Based on (8), it can be known that the relationship between V_o/V_{cm1} and d_{on} is hardly expressed clearly. The main reason is that there is a dead time of the input current, which causes the existence of α . If V_{cm1} is not enough compared with V_M , α can be ignored. Thus, it gives a simplified expression.

The average current $i_{D1,avg}$ of the diode D_1 is

$$i_{D1,avg} = \frac{[V_M \sin(\omega t) - V_{cm1}]^2 d_{on}^2}{2V_{cm1} L_1 f_s} \quad (9)$$

Considering the voltage balance of C_{m1} , it has

$$\frac{1}{T_L/2} \int_0^{T_L/2} i_{D2,avg} dt = \frac{1}{T_L/2} \int_0^{T_L/2} i_{D1,avg} dt \quad (10)$$

Thus, based on (5),(7), (9), and (10), it leads to

$$\frac{1}{2m_2^2} - \frac{2}{m_2 \pi} \frac{V_o}{V_M} - \frac{(2m_2 - 1)L_1}{2m_2 L_{p1}} \left(\frac{V_o}{V_M}\right)^2 = 0 \quad (11)$$

Based on (11), the voltage gain V_o/V_M can be expressed as

$$\frac{V_o}{V_M} = \frac{\frac{2}{\pi} + \sqrt{\frac{4}{\pi^2} + \frac{K_2}{m_2}}}{K_2} \quad (12)$$

where $K_2=(2m_2-1)L_1/L_{p1}$.

Based on the design parameters L_{p1} , f_s , and R_L given in Tab. I and (12), Fig. 7 gives the theoretical voltage gain with d_{on} as a variable. It can be seen that the higher inductance of L_1 can result in a higher voltage step-down ratio with the same d_{on} . Since large inductance usually means a larger size of an inductor, here $L_1=22 \mu$ H is chosen as given in Tab. I. However, since the dead time of the input current is ignored, it means that relatively larger d_{on} is actually used in the converter, which implies $d_{on}>0.035$, when $V_o=5$ V and $V_M=200$ V.

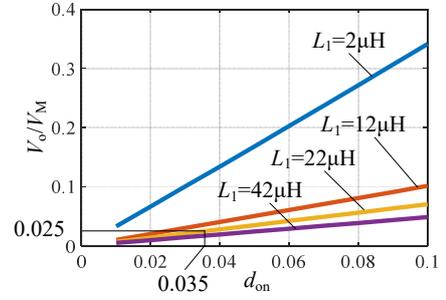


Fig. 7. Voltage gain of the proposed converter with L_1 as a variable.

III. SIMULATION VALIDATIONS

The proposed bridgeless quadratic buck converter circuit in IPOS configuration is built in PSIM for simulation verification with the parameters in Tab. I. A single-voltage closed-loop control is adopted to achieve the 200Vac to 5V voltage conversion. The AC input frequency is 300Hz to mimic an EH generator output waveform [22]. Note that the AC input frequency can be also set to other frequencies (e.g., 50Hz, 200Hz) and the proposed circuit is not sensitive to the AC input frequency as long as it is much lower than the switching frequency. The critical component simulation waveforms are shown in Fig. 8.

It can be seen in Fig. 8(b) that the output voltage is stable at 5V with a peak input voltage as high as 200Vac, which explains that the high voltage step-down ratio is achieved in the proposed converter. Specifically, the AC input voltage v_{in} is firstly converted to a middle voltage $V_{cm1}=V_{cm2}\approx 45$ V, and then V_{cm1} and V_{cm2} is further step-down to output voltage.

Besides, critical components operate only in each AC input cycle, which verify the bridgeless operation as demonstrated in Fig. 6. The waveforms in switching cycles during the positive and negative AC input cycle periods are also presented in Fig. 8(a) and (c). It shows that the inductors operate in DCM. The simulation waveforms imply that the proposed circuit operates well under the control loop and achieves the desired output.

The on-state duty cycle $d_{on} \cdot T_S$ is measured as 0.89μ s, i.e., $d_{on}=0.059$, which is slightly larger than the theoretical d_{on} in Fig. 7. The reason is that for simplification, the dead time of the input current is ignored. Thus, the slightly larger d_{on} is expected in the simulation. Fig. 9 shows the dead time of the input current in the simulation. Although the dead time is not large, zero power is processed during these time periods, leading to slightly larger duty cycle to achieve the same power conversion. Note that the dead time issue is commonly-seen in the buck-type AC-DC converters [17], which may takes topology modifications to eliminate is. However, since the AC-DC circuit in this application is not connected to the grid, the harmonics caused by the dead time is not as important as the circuit efficiency. Thus, the dead time issue in the proposed circuit is acceptable.

IV. CONCLUSION

Based on a quadratic buck converter cell, this paper proposes two high step-down bridgeless quadratic buck topologies as the interface circuit of TENGs. The proposed circuits use the quadratic buck cells to achieve the bridgeless operation with a high step-down voltage capability, which can handle the high output voltage of a TENG. Moreover,

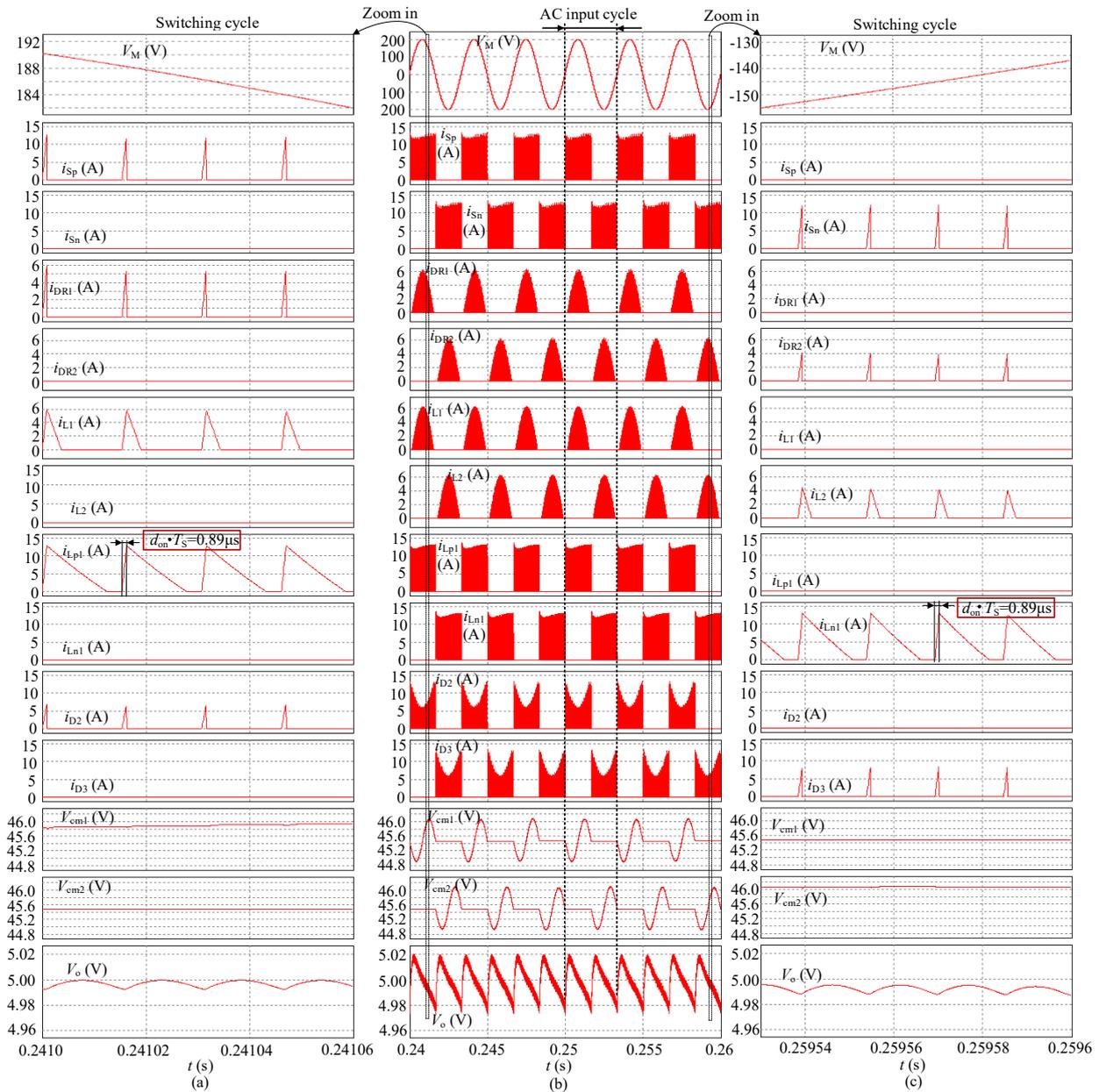


Fig. 8. Key waveforms of the proposed IPOS quadratic buck converter in switching cycle during (a) positive and (c) negative AC input cycles. (b) Waveforms in AC input cycles

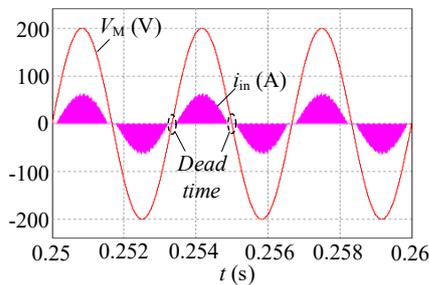


Fig. 9. Input current and voltage of the proposed converter.

they eliminate the rectifier diodes and the corresponding conduction loss. One specific topology is studied, along with its specific high voltage step-down ratio expression, and then the simplified voltage gain ratio under different input inductor parameters is presented to optimize the high voltage step-down capability. Finally, simulations are given, which verify the effectiveness of the proposed circuit and the correctness

of the theoretical voltage gain analysis. Power loss analysis, input voltage fluctuation impact, and performance comparison with other converters will be given in the future work.

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